AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

Accordingly, it is a feature of the present invention to provide an apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor via an external instruction bus. The apparatus includes instruction translation logic and bypass logic. The instruction translation logic retrieves macro instructions provided via the external instruction bus, and decodes each of the macro instructions into associated native instructions for execution by the microprocessor, wherein the instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions, and wherein the memory address is explicitly prescribed by contents of an architectural register, the contents and the architectural register being prescribed by a macro instruction. The bypass logic is coupled to the instruction translation logic. The bypass logic disables the instruction translation logic upon detection of the native bypass macro instruction, and provides the programmed native instructions directly to execution logic for execution ~~for execution by the microprocessor~~, thereby bypassing the instruction translation logic.

In another aspect, it is a feature of the present invention to provide an apparatus that allows a micro instruction to be directly provided from an external instruction bus to execution logic within a pipeline microprocessor. The apparatus has a translator and bypass logic. The translator receives macro instructions from a macro instruction bus, and translates each of the macro instructions into associated micro instructions, where the associated micro instructions are provided directly to the execution logic via a micro instruction bus, and where the translator translates a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the micro instruction, and where the memory address is explicitly prescribed by contents of an architectural register. The contents the

architectural register are prescribed by a macro instruction. The bypass logic is coupled to the translator. The bypass logic routes the micro instruction directly to the execution logic. The bypass logic includes a mode detector and native instruction routing logic. The mode detector detects the native bypass macro instruction, and directs that the translator cease instruction translation. The native instruction routing logic is coupled to the mode detector. The native instruction routing logic receives the micro instruction from the macro instruction bus, and provides the micro instruction directly to the execution logic via saidto the micro instruction bus, thereby circumventing the translator.

In a further aspect, it is a feature of the present invention to provide a microprocessor for executing micro instructions directly from memory. The microprocessor includes translation logic, mode detection logic, and an instruction router. The translation logic receives macro instructions from the memory, and decodes the macro instructions into corresponding micro instructions for execution by the microprocessor. The mode detection logic is coupled to the translation logic. The mode detection logic detects bypass macro instructions, and directs the microprocessor to execute the micro instructions directly from the memory rather than via the translation logic. The bypass macro instructions include a native branch macro instruction and a native branch return macro instruction. The native branch macro instruction directs that program control be transferred to a target address, where the translation logic decodes the native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to the target address, and where the target address contains the micro instructions, and where the target address is explicitly prescribed by contents of an architectural register. The contents and the architectural register are prescribed by a macro instruction. The native branch return macro instruction directs that program control be transferred to a return address. The instruction router is coupled to the mode detection logic. The instruction router receives the micro instructions, and routes the micro instructions directly to execution logic, thereby bypassing the translation logic.